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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO.
09/955,230	09/18/2001	Christopher J. Kelly	INTL-0644-US (P12307)	8306

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EXAMINER	
DINH, TUAN T	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 10/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,230	KELLY ET AL.	
	Examiner	Art Unit	
	Tuan T Dinh	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on 06 February 2003 is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

The office action mailed on 06/03/03 is hereby withdrawn.

Claim Objections

Claim 17 is objected to because of the following informalities:

Claim 17, line 3, "the signal layer" is unclear. Examiner suggests to change " the signal layer" to –a signal layer--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkman (U. S. Patent 6,064,113) in view of Nuxoll et al. (U. S. Patent 6,307,769).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

As to claims 1, 3-5, Kirkman discloses a printed circuit board (substrate 42 of a package 40-figure 2, column 5, line 56) as shown in figures 2-5 comprising:

a signal layer (80-figure 3, column 7, line 14) comprising traces (66, 68, column 6, lines 26-27) to communicate signals not associated with regulated supply voltage; and

a supply voltage plane (46, 48, column 5, lines 62-63) having an outer boundary, lies substantially within a region located directly below a component (die 62-figure 3) and embedded in the signal layer (80) to supply power of the component (die 62-figure 3) mounted to the printed circuit board (42).

Kirkman does not disclose the component having a multiple pins connected to the PCB. Nuxoll shows a PCB (31,column 9, line 47) in figures 3A-3C comprising a component (33, 35, column 9, lines 50-52) having supply voltage pins (column 10, lines 5-33) mounted to the PCB.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a component having supply voltage pins in the PCB of Kirkman, as taught by Nuxoll et al., for the purpose of providing inputs/outputs of power and ground signal terminals to the PCB.

As to claims 2, 6-7, Kirkman discloses the PCB in figure 3 further comprising a supply voltage plane layer (84, column 7, line 42) separate from the signal layer (80), and the supply voltage plane layer (84) comprises an embedded ground plane (90, column 7, lines 41-42) to provide ground connections (solder balls, see figure 3) for the signal layer (80), the ground connections associated with electrical devices (not shown) connected to the component.

As to claims 8-11, Kirkman discloses the PCB as shown in figure 3 wherein the ground plane (90) having an outer boundary and larger than the supply voltage plane. The ground plane lies substantially within a region located directly below the component.

As to claim 12, Kirkman discloses the PCB as show in figure 3 further comprising:

a core layer (300, see the attached paper),

wherein the signal layer (80) and the supply voltage plane layer (84) are located on the same side of the core layer.

As to claims 13-14, Kirkman discloses the PCB as shown in figures 2-5 wherein the supply voltage and the ground plane, each reduces and inductance.

As to claims 15, 17-19, Kirkman discloses a printed circuit board (42, see figures 2-3) comprising:

a supply voltage plane layer (84) to communicate a supply voltage; and

a ground plane (90) embedded in the supply voltage plane layer (84), the ground plane has an outer boundary, locates directly below a component (die 62), associates with electrical devices (not shown), and provides ground connections (by ground vias) to the component (62) mounted on the printed circuit board.

Kirkman does not disclose the component having a multiple pins connected to the PCB. Nuxoll et al. shows a PCB (31) in figures 3A-3C comprising a component (33, 35) having multiple pins mounted to the PCB.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a component having multiple pins in the PCB of Kirkman, as taught by Nuxoll et al., for the purpose of providing grounding connection between the component to the PCB.

As to claim 16, Kirkman discloses the PCB as shown in figure 3 further comprising: a ground plane layer (82) separate from the supply voltage plane layer (260).

Regarding claims 20-29, the method is necessitated by the PCB structure as discloses by Kirkman in view of Nuxoll et al. in claims 1-19.

Response to Arguments

3. Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fusaro et al. and Kakimoto et al. disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703-308-1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0658.

Tuan Dinh
September 30, 2003.